



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,100	08/26/2003	Shuji Fujimoto	16869S-092200US	4948

20350 7590 12/14/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER

MANOSKEY, JOSEPH D

ART UNIT PAPER NUMBER

2113

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/649,100

Applicant(s)

FUJIMOTO, SHUJI

Examiner

Joseph D. Manoskey

Art Unit

2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 8/26/03, 10/6/03, 4/24/05
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Venkatesh et al., U.S. Patent 6,397,292, hereinafter referred to as "Venkatesh".

3. Referring to claim 1, Venkatesh teaches a data storage device controller that contains redundant processor channel adapters that interface with host processors that connect to two mirror disk arrays, this is interpreted as a storage device controller comprising channel control portions each including a circuit board on which a file access processing portion for receiving file-by-file data input/output requests sent from information processors and an I/O processor for outputting I/O requests corresponding to said data input/output requests to storage devices are formed, said channel control portions being classified into groups for the sake of fail-over (See Fig. 3 and Col. 4, lines 47-55).

Venkatesh also teaches storage controller having dual redundant data paths and multiple redundant processors in the event of a failure to single path failure, and the disks can be accessed by either channel adapters, this is interpreted as processing portion configured to decide that data updated by each of said channel control portions and handed over at the time of said fail-over are stored in a shared volume which is a storage region logically set on physical storage regions provided by said storage devices and which can be accessed commonly by any other channel control portion belonging to the same group as said channel control portion updating said data (See Fig. 3, and Col. 4, lines 47-55).

4. Referring to claim 2, Venkatesh teaches a data storage device controller that contains redundant processor channel adapters that interface with host processors that connect to two mirror disk arrays, this is interpreted as a storage device controller comprising channel control portions each including a circuit board on which a file access processing portion for receiving file-by-file data input/output requests sent from information processors and an I/O processor for outputting I/O requests corresponding to said data input/output requests to storage devices are formed, said channel control portions being classified into groups for the sake of fail-over (See Fig. 3 and Col. 4, lines 47-55).

Venkatesh also teaches the channel adapters having a shared memory for cache memory, this is interpreted as a processing portion configured to decide that data updated by each of said channel control portions and handed over at the time of said

fail-over are stored in a shared memory which is contained in said storage device controller and which can be accessed commonly by said channel control portions (See Fig. 3 and Col. 4, lines 55-61).

5. Referring to claim 3, Venkatesh teaches a data storage device controller that contains redundant processor channel adapters that interface with host processors that connect to two mirror disk arrays, this is interpreted as a storage device controller comprising channel control portions each including a circuit board on which a file access processing portion for receiving file-by-file data input/output requests sent from information processors and an I/O processor for outputting I/O requests corresponding to said data input/output requests to storage devices are formed, said channel control portions being classified into groups for the sake of fail-over (See Fig. 3 and Col. 4, lines 47-55).

Venkatesh also teaches the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as a processing portion configured to decide that data updated by each of said channel portions and handed over at the time of said fail-over are sent to another channel control portion belonging to the same group as said channel control portion updating said data, through a network connecting said channel portions to one another (See Fig. 3, and Col. 4, lines 30-36).

6. Referring to claim 4, Venkatesh discloses the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as local volumes which are storage regions logically set on said physical storage regions provided by said storage devices and which can be accessed by said channel control portions individually and respectively are assigned to said channel control portions respectively and said processing portion further decides that said data are stored in said local volume of the other channel control portion belonging to the same group as said channel control portion updating said data (See Fig. 3, and Col. 4, lines 30-36).

7. Referring to claim 5, Venkatesh also teaches the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as local volumes which are storage regions logically set on said physical storage regions provided by said storage devices and which can be accessed by said channel control portions individually and respectively are assigned to said channel control portions respectively and said processing portion further decides that said data are stored in said local volume of the other channel control portion belonging to the same group as said channel control portion updating said data (See Fig. 3, and Col. 4, lines 30-36).

Venkatesh also teaches the channel adapters having a shared memory for cache memory and cache index, this is interpreted as said storage device controller further comprises an inherited data reference table on which reference destinations of said

data are recorded and said processing portion reads said data from any one of said shared volume, said shared memory and said local volumes on the basis of said reference destinations of said data recorded in said inherited data reference table (See Fig. 3 and Col. 4, lines 55-61).

8. Referring to claim 6, Venkatesh discloses the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as wherein said processing portion sends said data to all said channel control portions in said storage device controller through said network when said data are shared data allowed to be referred to by all said channel control portions in said storage device controller (See Fig. 3, and Col. 4, lines 30-36).

9. Referring to claim 7, Venkatesh teaches the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as wherein said processing portion stores said data in a second shared volume which is a storage region logically set on physical storage regions provided by said storage devices and which can be accessed commonly by all said channel control portions in said storage device controller when said data are shared data allowed to be referred to by all said channel control portions in said storage device controller (See Fig. 3, and Col. 4, lines 30-36).

10. Referring to claim 8, Venkatesh discloses the server being configured to be a network file server, this is interpreted as wherein said data handed over at the time of said fail-over contain at least one of NFS user data, CIFS user data, system administrator data, fail-over heart beat, IP address of a channel control portion, NFS file lock information and cluster control information (See Col. 5, lines 20-22).

11. Referring to claim 9, Venkatesh teaches a method of using a data storage device controller that contains redundant processor channel adapters that interface with host processors that connect to two mirror disk arrays, this is interpreted as a control method for a storage device controller including channel control portions each including a circuit board on which a file access processing portion for receiving file-by-file data input/output requests sent from information processors and an I/O processor for outputting I/O requests corresponding to said data input/output requests to storage devices are formed, said channel control portions being classified into groups for the sake of fail-over (See Fig. 3 and Col. 4, lines 47-55).

Venkatesh also teaches storage controller having dual redundant data paths and multiple redundant processors in the event of a failure to single path failure, and the disks can be accessed by either channel adapters, this is interpreted as deciding that data updated by each of said channel control portions and handed over at the time of said fail-over are stored in a shared volume which is a storage region logically set on physical storage regions provided by said storage devices and which can be accessed

commonly by any other channel control portion belonging to the same group as said channel control portion updating said data (See Fig. 3, and Col. 4, lines 47-55).

12. Referring to claim 10, Venkatesh teaches a method of using a data storage device controller that contains redundant processor channel adapters that interface with host processors that connect to two mirror disk arrays, this is interpreted as a control method for a storage device controller comprising channel control portions each including a circuit board on which a file access processing portion for receiving file-by-file data input/output requests sent from information processors and an I/O processor for outputting I/O requests corresponding to said data input/output requests to storage devices are formed, said channel control portions being classified into groups for the sake of fail-over (See Fig. 3 and Col. 4, lines 47-55).

Venkatesh also teaches the channel adapters having a shared memory for cache memory, this is interpreted as a deciding that data updated by each of said channel control portions and handed over at the time of said fail-over are stored in a shared memory which is contained in said storage device controller and which can be accessed commonly by said channel control portions (See Fig. 3 and Col. 4, lines 55-61).

13. Referring to claim 11, Venkatesh teaches a method of using a data storage device controller that contains redundant processor channel adapters that interface with host processors that connect to two mirror disk arrays, this is interpreted as a control method for a storage device controller comprising channel control portions each

including a circuit board on which a file access processing portion for receiving file-by-file data input/output requests sent from information processors and an I/O processor for outputting I/O requests corresponding to said data input/output requests to storage devices are formed, said channel control portions being classified into groups for the sake of fail-over (See Fig. 3 and Col. 4, lines 47-55).

Venkatesh also teaches the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as a sending data updated by each of said channel portions and handed over at the time of said fail-over are sent to another channel control portion belonging to the same group as said channel control portion updating said data, through a network connecting said channel portions to one another (See Fig. 3, and Col. 4, lines 30-36).

14. Referring to claim 12, Venkatesh discloses the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as local volumes which are storage regions logically set on said physical storage regions provided by said storage devices and which can be accessed by said channel control portions individually and respectively are assigned to said channel control portions respectively and said processing portion further decides that said data are stored in said local volume of the other channel control portion belonging to the same group as said channel control portion updating said data (See Fig. 3, and Col. 4, lines 30-36).

15. Referring to claim 13, Venkatesh also teaches the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as local volumes which are storage regions logically set on said physical storage regions provided by said storage devices and which can be accessed by said channel control portions individually and respectively are assigned to said channel control portions respectively and storing said data in said local volume of the other channel control portion belonging to the same group as said channel control portion belonging to the same group as said channel control portion updating said data (See Fig. 3, and Col. 4, lines 30-36).

Venkatesh also teaches the channel adapters having a shared memory for cache memory and cache index, this is interpreted as referring to an inherited data reference table on which reference destinations of said data are recorded and reading said data from any one of said shared volume, said shared memory and said local volumes on the basis of said reference destinations of said data recorded in said inherited data reference table (See Fig. 3 and Col. 4, lines 55-61).

16. Referring to claim 14, Venkatesh discloses the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as further comprising sending said data to all said channel control portions in said storage device controller through said network when said data are shared data allowed to be referred to by all said channel control portions in said storage device controller (See Fig. 3, and Col. 4, lines 30-36).

17. Referring to claim 15, Venkatesh teaches the disk arrays being mirrored so that the second disk array contains a copy of all the data from the first disk array, this is interpreted as further comprising storing said data in a second shared volume which is a storage region logically set on physical storage regions provided by said storage devices and which can be accessed commonly by all said channel control portions in said storage device controller when said data are shared data allowed to be referred to by all said channel control portions in said storage device controller (See Fig. 3, and Col. 4, lines 30-36).

18. Referring to claim 16, Venkatesh discloses the server being configured to be a network file server, this is interpreted as wherein said data handed over at the time of said fail-over contain at least one of NFS user data, CIFS user data, system administrator data, fail-over heart beat, IP address of a channel control portion, NFS file lock information and cluster control information (See Col. 5, lines 20-22).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are closely related storage device controller systems.

U.S. Patent 5,155,845 to Beal et al.

U.S. Patent 5,544,347 to Yanai et al.

U.S. Patent 5,574,863 to Nelson et al.

U.S. Patent 5,720,028 to Matsumoto et al.

U.S. Patent 5,774,643 to Lubbers et al.

U.S. Patent 6,401,223 to DePenning

U.S. Patent 6,523,138 to Natsume et al.

U.S. Patent App. Pub. 2001/0004754 to Murayama

U.S. Patent App. Pub. 2003/0135782 to Matsunami et al.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/649,100
Art Unit: 2113

Page 13

JDM
December 10, 2005


ROBERT BEAUSOLEIL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2103